

ABSTRACT

An integrated chip package structure and method of manufacturing the same is by adhering dies on a silicon substrate and forming a thin-film circuit layer on top of the dies and the silicon substrate. Wherein the thin-film circuit layer has an external circuitry, which is electrically connected to the metal pads of the dies, that extends to a region outside the active surface of the dies for fanning out the metal pads of the dies. Furthermore, a plurality of active devices and an internal circuitry is located on the active surface of the dies. Signal for the active devices are transmitted through the internal circuitry to the external circuitry and from the external circuitry through the internal circuitry back to other active devices. Moreover, the chip package structure allows multiple dies with different functions to be packaged into an integrated package and electrically connecting the dies by the external circuitry.

1006555-0132